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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 20

Application Number: 08/922,300
Filing Date: September 02, 1997
Appellant(s): PARK, GEUN-WOO

Robert E. Bushnell & Law Firm
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 8/13/01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claim 1 stands or falls alone and claims 2-11 stand or fall together with claim 1 because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

Description of Prior Art (BACKGROUND OF THE INVENTION) page 1 line 17-page 4 line 5; and

3,555,348	Van Clifton Martin	1/1971

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art in view of Van Clifton Martin (U.S. Patent No. 3,555,348).

In regard to claims 1 and 4, Applicant discloses in the background of the invention:

- a pulse width modulation (PWM) controller for generating a PWM signal under the control of the microcomputer;
- a current amplifier for amplifying current in response to the PWM signal from the PWM controller;

- a horizontal/vertical(H/V) processor for driving a horizontal driver under the control of a microcomputer;
- the H/V processor outputs a horizontal pulse signal of square wave to the horizontal driver under the control of a microcomputer;
- a horizontal deflection coil is mounted to the next of a display device so that electron beams can be deflected to the left or right according to a direction of current flowing through the coil;
- an S-correction capacitor applies a parabola voltage to the horizontal deflection coil to correct a linearity of center-to-left and right sides of a screen of the display device;
- a horizontal output circuit for supplying current to a horizontal deflection coil and an S-correction capacitor in response to output signals from the current amplifier and horizontal driver;
- a horizontal/vertical (H/V) processor constant voltage circuit for supplying a constant voltage to the H/V processor to drive it;

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage –V1 from the power supply by a diode 44 connected between voltage-V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22

thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the voltage at the control grid 14 drop slowly even thought its bias voltage –V1 is removed** (see col. 2 lines 64-72).

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions of circuits to the tube (see Van Clifton Martin col. 1 lines 36-39).

In regard to claim 3, Applicant admitted prior art discloses:

- a power supply circuit is adapted to convert commercial alternating current (AC) into direct current (DC) (see page 2 of the background of the invention lines 1-2);
- a horizontal deflection circuit under the control of a microcomputer, receiving said direct current input voltage, for horizontally deflecting electron beams generated in the cathode ray tube (see page 2 background of the invention lines 5-8)

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said direct current input. In addition, Applicant's admitted prior art does not disclose a polarity capacitor and a diode connected to said polarity capacitor.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage –V1 from the power supply by a diode 44 connected between voltage-V1 and the control grid 14 and a capacitor 45 connected

between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the voltage at the control grid 14 drop slowly even thought its bias voltage –V1 is removed** (see col. 2 lines 54-72).

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions of circuits to the tube (see Van Clifton Martin col. 1 lines 36-39).

In regard to claims 5 and 8, Applicant admitted prior art discloses in Fig. 2 and background of the invention:

- a pulse width modulation (PWM) controller for generating a PWM signal under the control of the microcomputer;
- a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;
- a current amplifier transformer having a primary coil and a secondary coil (see T1);
- a field effect transistor having its gate terminal connected to one terminal of said secondary coil (see FET1);

- one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller 135 through a capacitor and another terminal of said primary coil being connected to the ground terminal;
- said field effect transistor having a drain terminal connected to a high voltage source B+ and a source terminal connected in common to a second terminal of said secondary coil and one other side of a pulse transformer PT;
- said pulse transformer having a second side connected to one side of said horizontal deflection coil;
- a first diode connected between said source terminal and said drain terminal;
- a second diode connected between said second terminal of said secondary coil and said ground terminal;
- a H/V processor for generating a square wave pulse signal under the control of said microcomputer;
- a horizontal driver 144 for generating drive pulse signal in response to the square wave pulse signal from said H/V processor;
- an S-correction capacitor applies a parabola voltage to the horizontal deflection coil to correct a linearity of center-to-left and right sides of a screen of the display device;
- a horizontal output circuit for supplying current to a horizontal deflection coil and an S-correction capacitor in response to output signals from the current amplifier and horizontal driver;

- a horizontal/vertical (H/V) processor constant voltage circuit for supplying a constant voltage to the H/V processor to drive it;

Applicant admitted prior art does not disclose a power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Van Clifton Martin discloses that the control grid 14 is clamped to a negative DC bias voltage –V1 from the power supply by a diode 44 connected between voltage-V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. **This diode-capacitor network makes the voltage at the control grid 14 drop slowly even thought its bias voltage –V1 is removed** (see col. 2 lines 64-72).

At the time of the invention, it would have been obvious to one skilled in the art to utilize Van Clifton Martin's protection circuit with Applicant admitted prior art because it would protect the CRT display in case of sudden failures or malfunctions of circuits to the tube (see Van Clifton Martin col. 1 lines 36-39).

In regard to claims 2 and 9, Van Clifton Martin discloses:

- a polarity capacitor for performing charging operation and a diode connected to the polarity capacitor for preventing a voltage on the polarity capacitor from being discharged (see col. 2 lines 64-72 and Fig. 1 element 45);

- a diode connected to said polarity capacitor for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supply to the display device is interrupted (see col. 2 lines 64-72 and Fig. 1 element 44).

In regard to claims 6 and 10, Applicant's admitted prior art discloses in Fig. 2 that said horizontal output circuit 234 comprises a horizontal output transistor TR having a collector terminal connected in common to said second side of said pulse transformer T2 and said one side of said horizontal deflection coil H-DY, an emitter terminal connected to said S-correction Capacitor Cs and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

In regard to claims 7 and 11, Applicant's admitted prior art discloses in Fig. 2:

- a second field effect transistor FET2 having a gate terminal connected to receive a square wave pulse signal from said horizontal/vertical processor 132, a source terminal connected to said ground terminal, and a drain terminal;
- a horizontal drive transformer T2 having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source V2 through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

- said secondary coil of said horizontal drive transformer T2 having one side connected to said base terminal or said horizontal output transistor 134 and a second side connected to said ground terminal.

(11) Response to Argument

Applicant argues the following:

- it is not obvious to combine Applicant admitted prior art with Van Clifton Martin for claims 1, 3 and 8;
- "Martin fails to teach or suggest, to one of ordinary skill in the art, gradually lowering the input voltage to a H/V processor constant voltage circuit when power supplied to the display device is interrupted".

Examiner disagrees with the applicant argument:

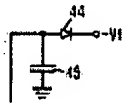
Claims 1-11 are obvious and unpatentable over the combined teachings of Applicant admitted prior art and Martin.

In regard to claims 1, 3, and 8, Applicant concedes that Applicant's admitted prior art (see Fig. 2; and Description of related art in the Background of the Invention) teaches all that is claimed except the feature of power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

Martin's discloses a protection circuit for a display device which ensures screen protection in case of sudden failures or malfunctions of circuits to the tube (see col. 1 lines 35-39), which ensures that the screen will not be damaged by a strong beam

current (see col. 1 lines 5-8). Martin specifically discloses : **" This diode-capacitor network makes the voltage at the control grid 14 drop slowly even thought its bias voltage –V1 is removed"** in col. 2 lines 63-72.

In other words not only does Martin teach the structure, the functionality of the circuit arrangement, Martin also applies the above circuit configuration to gradually or slowly lower the DC input voltage as claimed by applicant.

By incorporating Martin's power interruption delay charging circuit as depicted in Martin's Fig. 1, a portion of which is adjoined herein 

(which is a well known circuitry) including a voltage prevention diode 44, a capacitor 45, a bias voltage, into the prior art admitted by the Applicant in Fig. 2 one of the ordinary skill in the art can easily comes up with the Applicant's invention.

In order words Martin has the same structure as the claimed circuitry. It is seen that Martin's circuitry performs the same function as the circuitry claimed by applicant. it is therefore obvious that one of the ordinary skill in the art would be motivated to use the technique of a power interruption delay charging structure to lower voltages applied slowly in order to protect display apparatus from harmful effects such as power surges, electrical spikes, high beam currents, etc. Therefore, one can clearly see that the approach of gradually decreasing voltages is well known, thereby rendering applicant's claimed invention obvious, hence unpatentable.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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September 13, 2001

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